TPS7H3301-SP Sink and Source Radiation-Hardened 3-A DDR Termination Regulator With Built-In VTTREF Buffer

1 Features

- 5962R14288[1]:
  - Radiation Hardness Assurance (RHA) Qualified to Total Ionizing Dose (TID) 100 krad(Si)
  - Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), Single Event Burnout (SEB) Immune to LET = 65 MeV-cm^2/mg (See *Radiation Report* for Details)
  - SET, SEFI, SEU Immune to 65 MeV-cm^2/mg (See *Radiation Report* for Details)
- Supports DDR, DDR2, DDR3, DDR3LP, and DDR4 Termination Applications and is Compliant to JEDEC Standards
- Input Voltage: Supports a 2.5-V and 3.3-V Rail[2]
- Separate Low-Voltage Input (VLDOIN) Down to .9 V for Improved Power Efficiency[2]
- 3-A Sink and Source Termination Regulator Includes Droop Compensation
- Enable Input and Power-Good Output for Power Supply Sequencing
- VTT Termination Regulator
  - Output Voltage Range: 0.5 to 1.75 V
  - 3-A Sink and Source Current
  - ±20-mV Accuracy
- Integrated Precision Voltage Divider Network With Sense Input
- Remote Sensing (VOSNS)
- VTTREF Buffered Reference
  - VDDQ/2 ±1% Accuracy
  - ±10-mA Sink and Source Current
- Undervoltage Lockout (UVLO), and Overcurrent Limit (OCL) Functionality Integrated

2 Applications

- Single Board Computers, Solid-State Recorders, and Payload Applications Where DDR, DDR2, DDR3, and Low-Power DDR3 and DDR4 Memory are Used
- Ultra-Fast Transient Power Applications
- Available in Military (–55°C to 125°C) Temperature Range
- Engineering Evaluation (/EM) Components are Available[3]

3 Description

The TPS7H3301-SP is a TID and SEE radiation-hardened double data rate (DDR) 3-A termination regulator with built-in VTTREF buffer. The regulator is specifically design to provide a complete, compact, low-noise solution for space DDR termination applications such as single board computers, solid state recorders, and payload processing.

The TPS7H3301-SP supports and is compliant to DDR, DDR2, DDR3, DDR4, and associated low-power JEDEC specifications. The fast transient response of the TPS7H3301-SP VTT regulator allows for a very stable supply during read/write conditions. . During transients, the fast tracking feature of the VTTREF supply minimizes any voltage offset between VTT and VTTREF. To enable simple power sequencing, both an enable input and a power-good output (PGOOD) have been integrated into the TPS7H3301-SP. The PGOOD output is open-drain so it can be tied to multiple open-drain outputs to monitor when all supplies have come into regulation. The enable signal can also be used to discharge VTT during suspend to RAM (S3) power down mode.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7H3301-SP	CFP (16)	9.60 mm × 11.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Applicable to DDR2, DDR3, DDR3L and DDR4. For DDR, input voltage = 3.3-V nominal. V_{IN} is 2.95 to 3.5 V for DDR1 and $V_{LDOIN} > V_{TT}$ for all DDRs. For DDR2 3-A load condition, V_{IN} is 2.45 to 3.5 V. V_{IN} headroom: $V_{IN\_MIN} \geq V_{TT} + 1.5$ V.

(3) These units are intended for engineering evaluation only. They are processed to a noncompliant flow (that is, no burn-in, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

Standard DDR Application

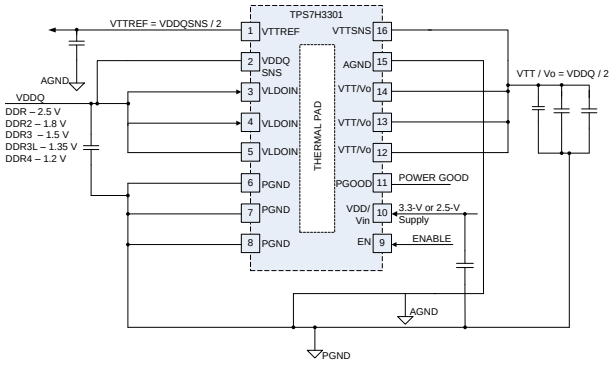


Table of Contents

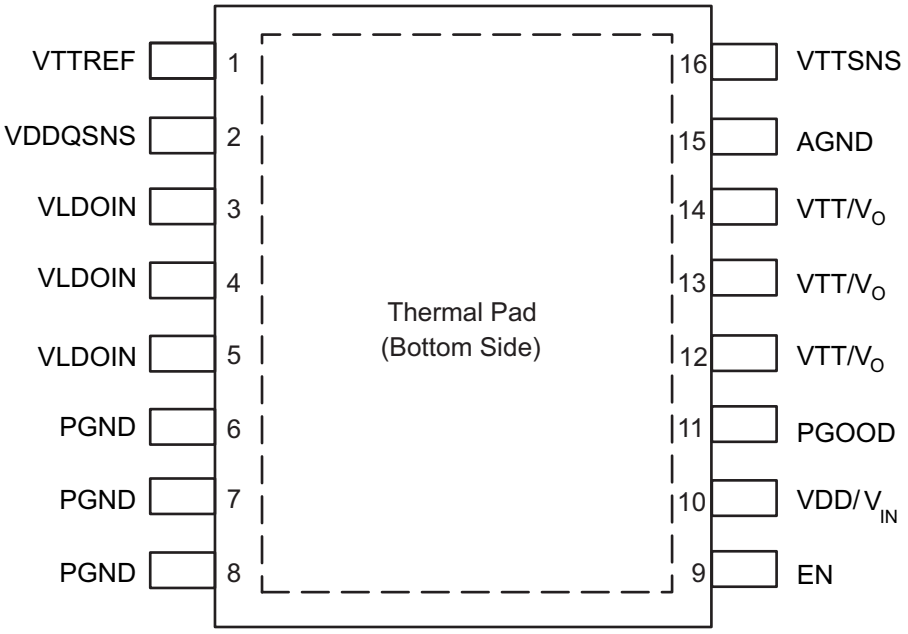
4 Revision History

Changes from Original (December 2015) to Revision A **Page**

- Changed title of data sheet ... 1
- Added new RHA device features ... 1
- Deleted soft start feature statement ... 1
- Deleted built-in VREF statement ... 1
- Deleted misplaced pin function ... 3
- Changed absolute maximum rating for EN pin to 3.6 V ... 4
- Deleted specification for PG pin sink current ... 4
- Deleted specification for peak output current ... 4
- Deleted unnecessary graphs from the *Typical Characteristics* section ... 7
- Changed typo for VTTREF disabling lower threshold from 0.375 to 0.76 V ... 11
- Edited content to reflect there is no built-in soft start and added details regarding tracking at startup ... 15

5 Pin Configuration and Functions

HKR Package
16-Pin CFP
Top View - Live Bug



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VTTREF	1	O	Reference output. Connect to GND through 0.1-µF ceramic capacitor.
VDDQSNS	2	I	VDDQ sense input. Reference input for VTTREF.
VLDOIN	3	I	Supply voltage for the LDO. Connect to VDDQ voltage or an alternate voltage source.
	4		
	5		
PGND	6	—	Power ground. Connect output for the VTT/V_O LDO to negative pin of the output capacitor.
	7		
	8		
EN	9	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.
VDD/V_{IN}	10	I	2.5- or 3.3-V power supply. A ceramic decoupling capacitor with a value between 1 and 10 µF is required.
PGOOD	11	O	PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.
VTT/V_O	12	O	Power output for VTT LDO.
	13		
	14		
AGND	15	—	Signal ground. Connect to negative pin of output capacitors.(1)
VTTSNS	16	I	Voltage sense for VTT/V_O. Connect to positive pin of the output capacitor or the load.

(1) Thermal pad and package lid are internally connected to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature, unless otherwise noted(1)

			MIN	MAX	UNIT
Input voltage(2)		V_{IN}/VDD, VLDOIN, VTTSNS, VDDQSNS	–0.36	3.6	V
		EN	–0.3	3.6	
		PGND to AGND	–0.3	0.3	
Output voltage(2)		V_O/VTT, VTTREF	–0.3	3.6	V
		PGOOD	–0.3	3.6	
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{IN}/VDD	2.375		3.5	V
Voltage	VLDOIN	0.9		3.5	V
	EN, VTTSNS	–0.1		3.5	
	VDDQSNS	1		3.5	
	V_O/VTT, PGOOD	–0.1		3.5	
	VTTREF	–0.1		1.8	
	PGND	–0.1		0.1	
T_J	Operating junction temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2) (3)		TPS7H3301-SP HKR (CFP) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(3) Maximum power dissipation may be limited by overcurrent protection.

6.5 Electrical Characteristics

Over full temperature range, –55°C to 125°C, V_{IN}/VDD = 3.3 V and 2.375 V, V_{VLDOIN} = 1.8 V, $V_{VDDQSNS}$ = 1.8 V, $V_{VOSNS/VTTSNS}$ = 0.9 V, V_{EN} = V_{IN}/VDD, *Standard DDR Application* (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}/I_{VDD}	Supply current	V_{EN} = 3.3 V, no load		18	30	mA
$I_{VDD(SDN)}$	Shutdown current	V_{EN} = 0 V, VDDQSNS = 0, no load		3	5	mA
		V_{EN} = 0 V, VDDQSNS > 0.78 V, no load		6.5	8	
I_{LDOIN}	Supply current of VLDOIN	V_{EN} = 3.3 V, no load		575	1200	µA
$I_{LDOIN(SDN)}$	Shutdown current of VLDOIN	V_{EN} = 0 V, no load		50	100	µA
INPUT CURRENT						
$I_{VDDQsns}$	Input current, VDDQsns	V_{EN} = 3.3 V		4	6	µA
V_O/V_{TT} OUTPUT						
$V_{VOSNS/VTTSNS}$	Output DC voltage, V_O	V_{LDOIN} = 2.5 V, V_{VTTREF} = 1.25 V (DDR1), I_O = 0 A		1.25		V
			–6		6	mV
		V_{LDOIN} = 1.8 V, V_{VTTREF} = 0.9 V (DDR2), I_O = 0 A		0.9		V
			–6		6	mV
		V_{LDOIN} = 1.5 V, V_{VTTREF} = 0.75 V (DDR3), I_O = 0 A		0.75		V
			–6		6	mV
		V_{LDOIN} = 1.35 V, V_{VTTREF} = 0.675 V (DDR3L), I_O = 0 A		0.675		V
			–6		6	mV
		V_{LDOIN} = 1.2 V, V_{VTTREF} = 0.6 V (DDR4), I_O = 0 A		0.6		V
			–6		6	mV
$V_{LDOIN} – V_{TT}$ (1)	$V_{LDOIN} > V_{TT}$	V_{IN}/V_{DD} = 2.95 V, $V_{VDDQSNS}$ = 2.5 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1), I_O = 0.5 A		50	230	mV
		V_{IN}/V_{DD} = 2.95 V, $V_{VDDQSNS}$ = 2.5 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1), I_O = 1 A		101	300	
		V_{IN}/V_{DD} = 2.95 V, $V_{VDDQSNS}$ = 2.5 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1), I_O = 2 A (2)		209	400	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.8 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2), I_O = 0.5 A (2)		54	230	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.8 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2), I_O = 1 A (2)		108	300	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.8 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2), I_O = 2 A (2)		228	400	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.5 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3), I_O = 0.5 A		52	230	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.5 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3), I_O = 1 A		104	300	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.5 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3), I_O = 2 A (2)		216	400	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.35 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3L), I_O = 0.5 A		50	230	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.35 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3L), I_O = 1 A		102	300	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.35 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3L), I_O = 2 A (2)		212	400	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.2 V, V_{TT} = V_{VTTREF} – 50 mV (DDR4), I_O = 0.5 A		50	230	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.2 V, V_{TT} = V_{VTTREF} – 50 mV (DDR4), I_O = 1 A		102	300	
		V_{IN}/V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.2 V, V_{TT} = V_{VTTREF} – 50 mV (DDR4), I_O = 2 A (2)		210	400	
$V_{VOTOL/VTTTOL}$	Output voltage tolerance to V_{VTTREF}	I_{VO} = –3 A, across V_{IN} voltage range (2)	12	25	34	mV
		I_{VO} = 3 A, across V_{IN} voltage range (2)	–34	–25	–12	
I_{VOSRCL}	V_O/VTT source current limit	With reference to V_{VTTREF}, V_{VTTSNS} = 90% × V_{VTTREF}	3.25		8	A

(1) Dropout and headroom information provided to help designer in optimizing system efficiency.
(2) Specified by characterization and not production tested.

Electrical Characteristics (continued)

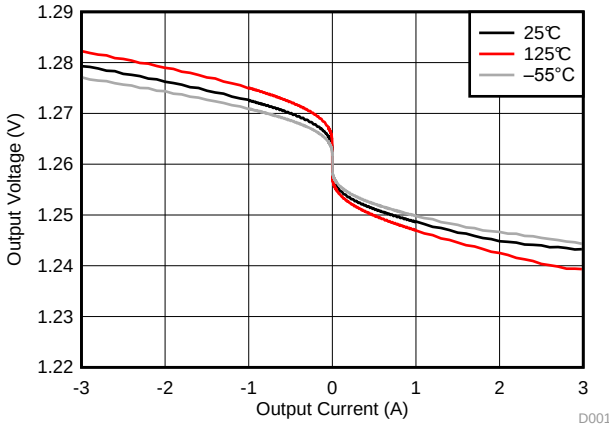
Over full temperature range, –55°C to 125°C, V_{IN}/VDD = 3.3 V and 2.375 V, V_{VLDOIN} = 1.8 V, $V_{VDDQSNS}$ = 1.8 V, $V_{VOSNS/VTTSNS}$ = 0.9 V, V_{EN} = V_{IN}/VDD, *Standard DDR Application* (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VOSNCL}	V_O/VTT sink current limit	With reference to V_{VTTREF}, V_{VTTSNS} = 110% × V_{VTTREF}	3.5		5.5	A
R_{DSCHRG}	Discharge impedance	V_{DDQSNS} = 0 V, V_{VO} = 0.3 V, V_{EN} = 0 V, T_A = 25°C		18	25	Ω
POWER-GOOD COMPARATOR						
$V_{TH(PG)}$	V_O/VTT PGOOD threshold	PGOOD window lower threshold with respect to V_{VTTREF}	–23.5%	–20%	–17.5%	
		PGOOD window upper threshold with respect to V_{VTTREF}	17.5%	20%	23.5%	
		PGOOD hysteresis		5%		
$T_{PGSTUPDLY}$	PGOOD startup delay	Startup rising edge, VOSNS within 15% of V_{VTTREF}		2		ms
$V_{PGOODLOW}$	Output low voltage	I_{SINK} = 4 mA			0.4	V
$T_{PBADDLY}$	PGOOD bad delay	V_{OSNS} is outside of the ±20% PGOOD window		1		µs
$I_{PGOODLK}$	Leakage current	V_{OSNS} = V_{REFIN} (PGOOD high impedance), PGOOD = V_{IN} + 0.2 V			1	µA
V_{DDQSNS} AND V_{VTTREF} OUTPUT						
V_{DDQSNS}	V_{DDQSNS} voltage range		1		2.8	V
V_{DDQSNS_UVLO}	V_{DDQSNS} undervoltage lockout	V_{DDQSNS} rising		780		mV
$V_{DDQSNSUVHYS}$	V_{DDQSNS} undervoltage lockout hysteresis			20		mV
V_{VTTREF}	V_{VTTREF} voltage			V_{DDQSNS} / 2		V
V_{VTTREF}	V_{VTTREF} voltage tolerance to $V_{VDDQSNS}$	–10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 2.5 V	–15		15	mV
		–10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.8 V	–15		15	
		–10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.5 V	–15		15	
		–10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.35 V	–15		15	
		–10 mA < I_{VTTREF} < 10 mA, $V_{VDDQSNS}$ = 1.2 V	–15		15	
$I_{VTTREFSRCL}$	V_{VTTREF} source current limit	VTTREF = 0 V	10	40		mA
$I_{VTTREFSNCCL}$	V_{VTTREF} sink current limit	VTTREF = 0 V	6	40		mA
$I_{VTTREFDIS}$	V_{VTTREF} discharge current	EN = 0 V, V_{DDQSNS} = 0 V, V_{VTTREF} = 0.5 V		1.3		mA
UVLO/EN LOGIC THRESHOLD						
$V_{VINUVVIN}$	UVLO threshold	Wakeup, T_A = 25°C		2.18	2.25	V
		Hysteresis		50		mV
V_{ENIH}	High-level input voltage	Enable	1.7			V
V_{ENIL}	Low-level input voltage	Enable			0.3	V
V_{ENYST}	Hysteresis voltage	Enable		0.5		V
I_{ENLEAK}	Logic input leakage current	EN, T_A = 25°C	–1		1	µA
THERMAL SHUTDOWN						
T_{SON}	Thermal shutdown threshold(3)	Shutdown temperature		210		°C
		Hysteresis		12		

(3) Ensured by design, not production tested.

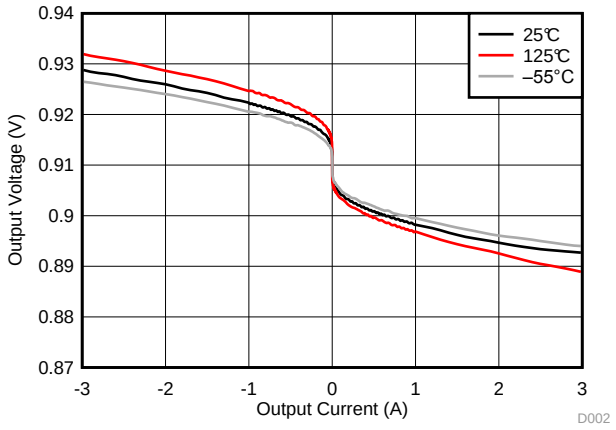
6.6 Typical Characteristics

For Figure 1 through Figure 10, (3 × 150-µF T530D157M010ATE005 tantalum + 4 × 4.7-µF MLCC) or equivalent capacitance/ESR are used on the output.



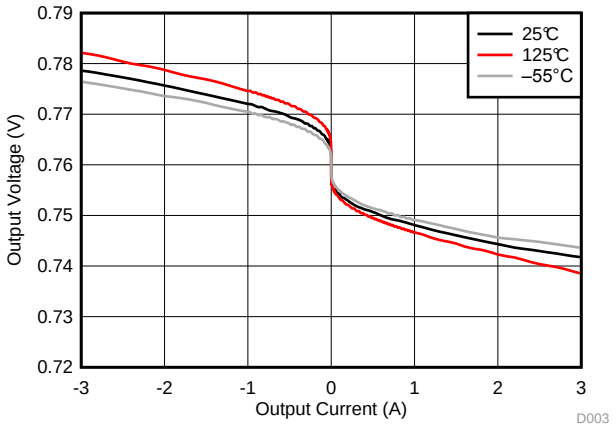
V_{IN} = 3.3 V VDDQSNS = 2.5 V

Figure 1. Output Voltage vs Output Current



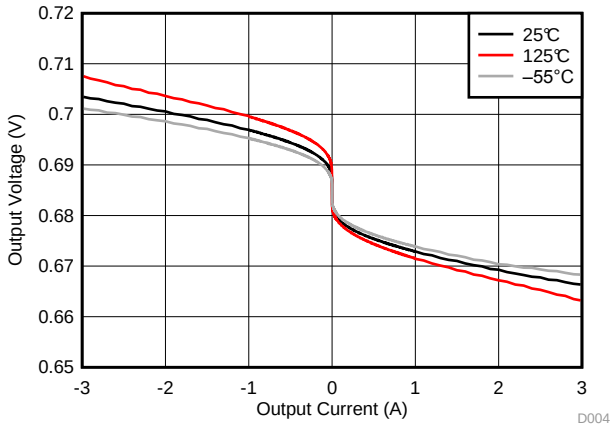
V_{IN} = 3.3 V VDDQSNS = 1.8 V

Figure 2. Output Voltage vs Output Current



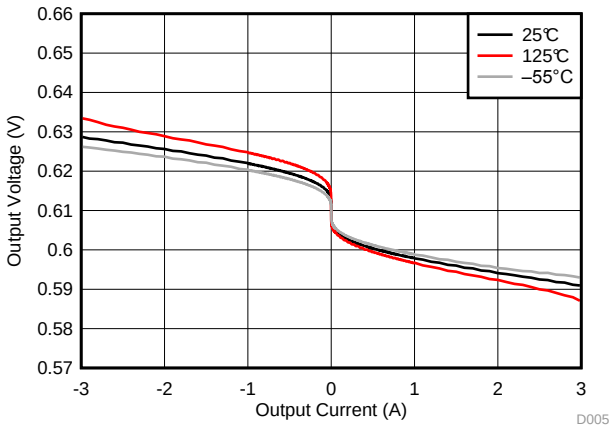
V_{IN} = 3.3 V VDDQSNS = 1.5 V

Figure 3. Output Voltage vs Output Current



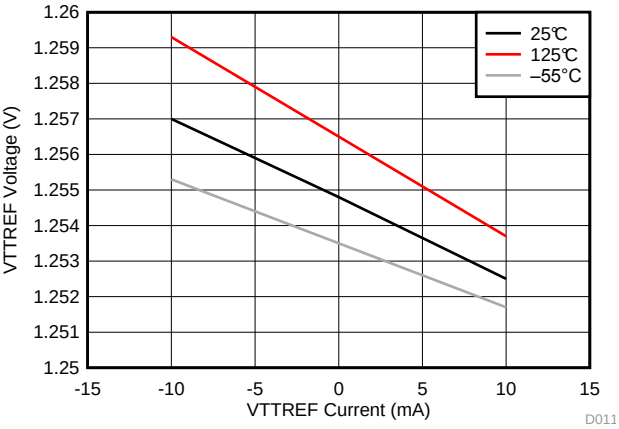
V_{IN} = 3.3 V VDDQSNS = 1.35 V

Figure 4. Output Voltage vs Output Current



V_{IN} = 3.3 V VDDQSNS = 1.2 V

Figure 5. Output Voltage vs Output Current

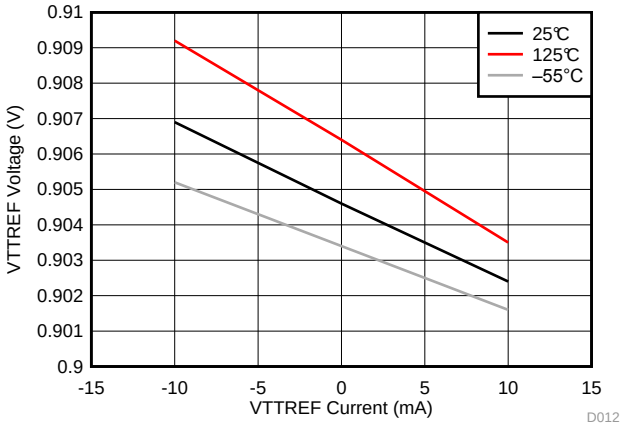


VDDQSNS = 2.5 V

Figure 6. RF Voltage vs REFOUT Current

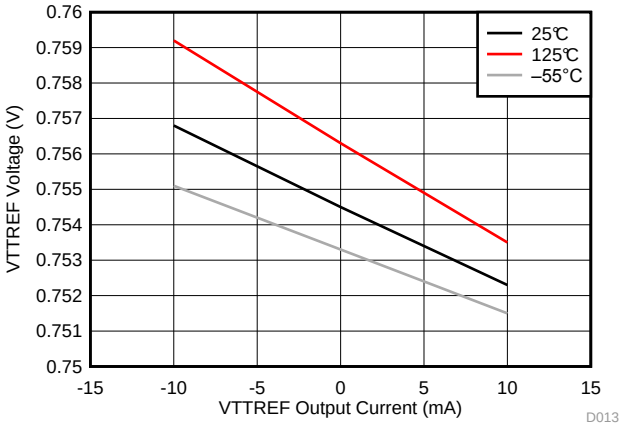
Typical Characteristics (continued)

For Figure 1 through Figure 10, (3 × 150-µF T530D157M010ATE005 tantalum + 4 × 4.7-µF MLCC) or equivalent capacitance/ESR are used on the output.



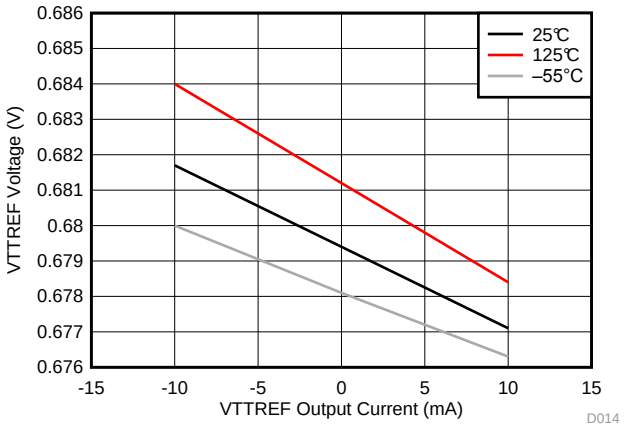
VDDQSNS = 1.8 V

Figure 7. RF Voltage vs REFOUT Current



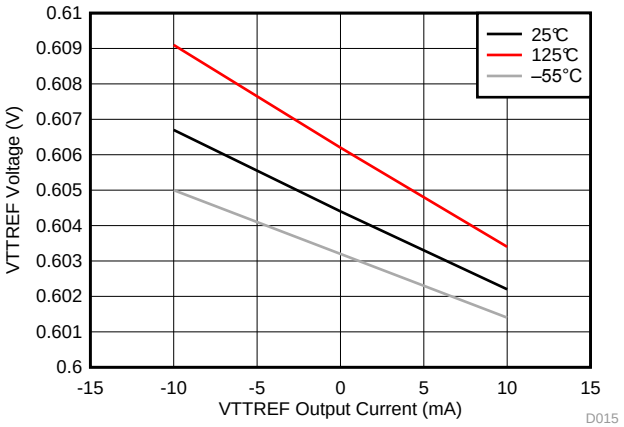
VDDQSNS = 1.5 V

Figure 8. RF Voltage vs REFOUT Current



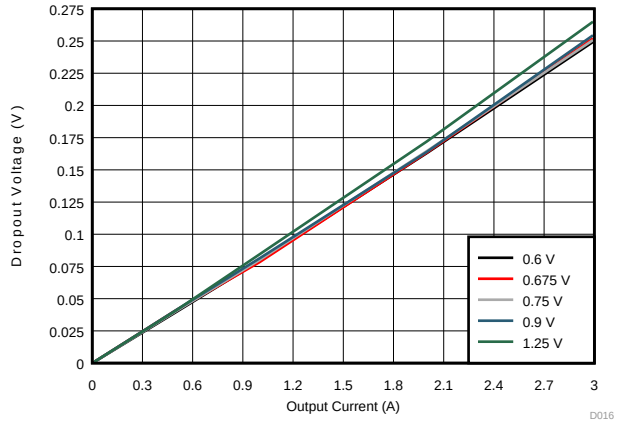
VDDQSNS = 1.35 V

Figure 9. RF Voltage vs REFOUT Current



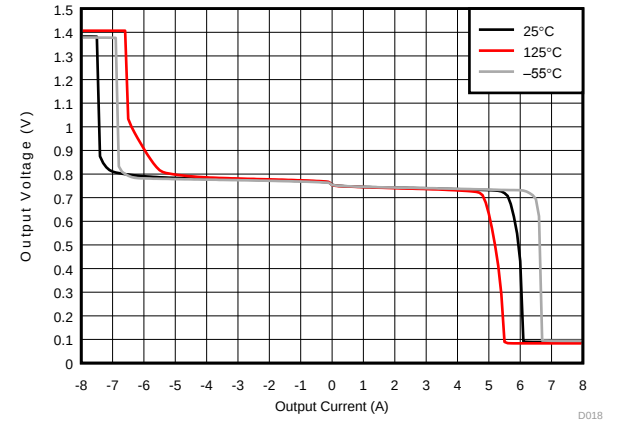
VDDQSNS = 1.2 V

Figure 10. RF Voltage vs REFOUT Current



V_{IN} = 3.6 V

Figure 11. Dropout Voltage vs Output Current

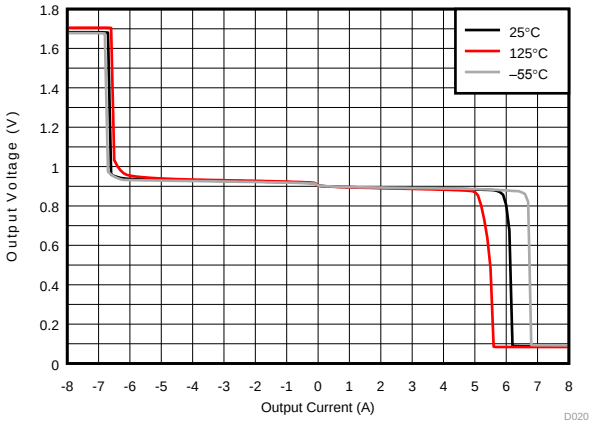


V_{IN} = 3.5 V VDDQSNS = 1.5 V

Figure 12. Output Voltage vs Output Current, DDR3

Typical Characteristics (continued)

For Figure 1 through Figure 10, (3 × 150-µF T530D157M010ATE005 tantalum + 4 × 4.7-µF MLCC) or equivalent capacitance/ESR are used on the output.



V_{IN} = 3.5 V VDDQSNS = 1.8 V

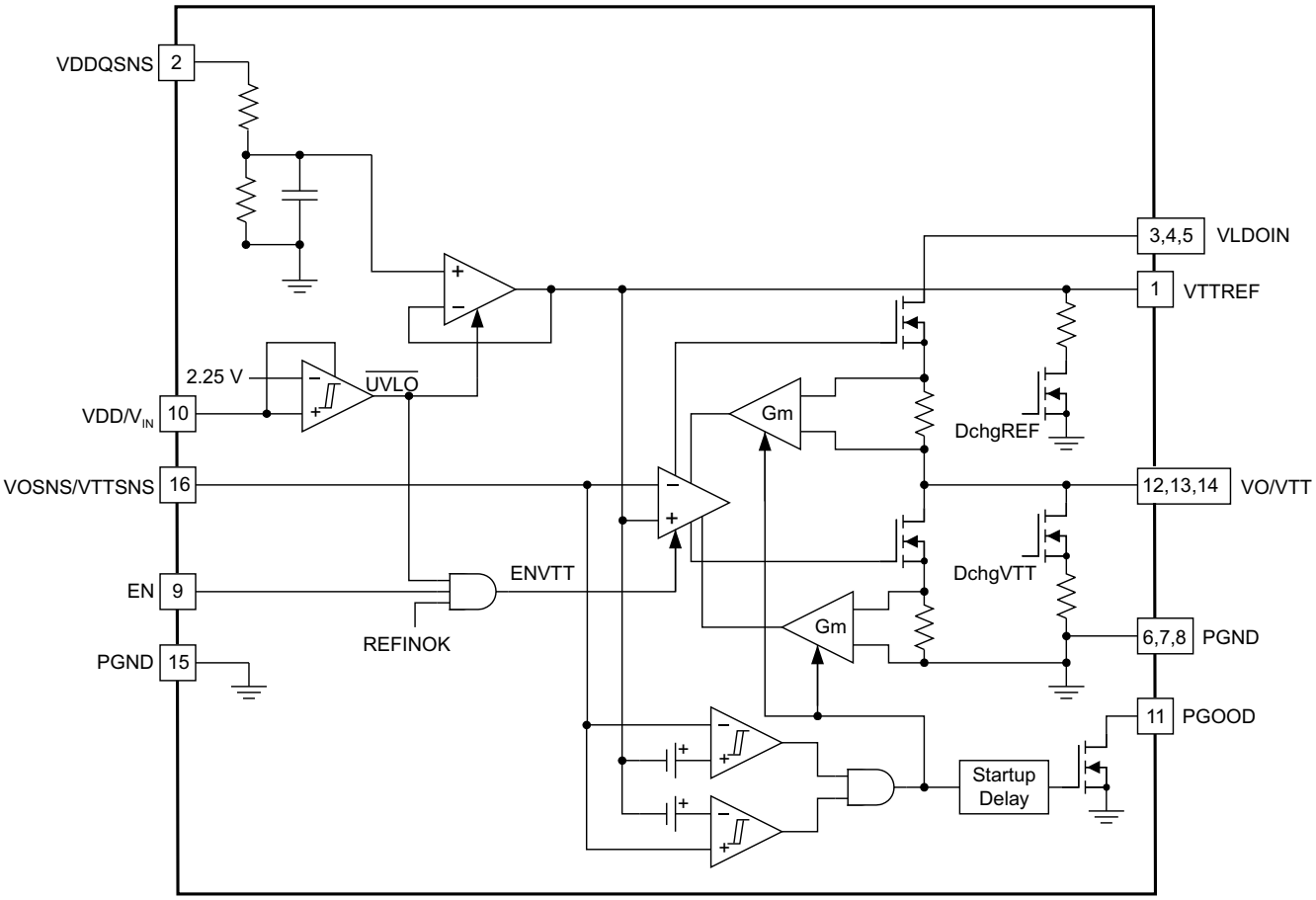
Figure 13. Output Voltage vs Output Current, DDR2

7 Detailed Description

7.1 Overview

The TPS7H3301-SP device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space and weight is a key consideration.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 V_O Sink and Source Regulator

The TPS7H3301-SP is a 3-A sink and source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems where space is a key application parameter. The TPS7H3301-SP integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sinking and sourcing current. The LDO regulator employs a fast feedback loop so that ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin (VOSNS/VTTSNS) should be connected to the positive pin of the output capacitor(s) as a separate trace from the high-current path of V_O/VTT.

The TPS7H3301-SP has a dedicated pin (VLDOIN) for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 400 mV above the 1/2 VDDQSNS voltage or as highlighted in *Electrical Characteristics* (VLDOIN to VTT headroom) for various load conditions.

Feature Description (continued)

7.3.2 Reference Input (VDDQSNS)

The output voltage, V_O/VTT, is regulated to VTTREF. VDDQSNS incorporates an integrated resistor divider network. VDDQSNS should be connected to the memory supply bus (VDDQ). The TPS7H3301-SP supports VDDQSNS voltage from 1 V to 3.5 V, making it versatile and ideal for many types of low-power LDO applications.

7.3.3 Reference Output (VTTREF)

When it is configured for DDR termination applications, VTTREF buffers the DDR VTT reference voltage for the memory application. VTTREF block consists of an on-chip 1/2 divider and a low-pass filter (LPF). VTTREF tracks 1/2 of VDDQSNS with 1% accuracy. It is capable of supporting both a sourcing and sinking load of 10 mA. VTTREF becomes active when VDDQSNS voltage rises to 0.78 V and V_{IN}/VDD is above the UVLO threshold. When VTTREF is less than 0.76 V, VTTREF is disabled and subsequently discharges to GND through an internal MOSFET. V_O/VTT is also discharged following the discharge of VTTREF. VTTREF is independent of the EN pin state. To meet stability criteria, a capacitor of 0.1-µF minimum must be installed close to VTTREF (pin1). Capacitor value at VTTREF (pin 1) must not exceed 2.2 µF.

7.3.4 EN ControL (EN)

When EN is driven high, the TPS7H3301-SP V_O/VTT regulator begins normal operation. When EN is driven low, V_O/VTT discharges to GND through an internal 18-Ω MOSFET. VTTREF remains on when EN is driven low. EN is not tied high internally to prevent power sequencing issues with an external signal that may be controlling the enable. EN is a floating input and not internally tied, thus the user can have complete control over where and when the EN signal is generated. EN feeds directly into power-good (PGOOD). When enable is low, PGOOD is low.

7.3.5 Power-Good Function (PGOOD)

The TPS7H3301-SP provides an open-drain PGOOD output that goes high when the V_O/VTT output is within 20% of VTTREF (typ). PGOOD deasserts within 1 µs after the output exceeds the size of the power-good window. During initial V_O/VTT startup, PGOOD asserts high 2 ms (typ) after the V_O/VTT enters power-good window. Because PGOOD is an open-drain output, a 100-kΩ pullup resistor between PGOOD and a stable active supply voltage rail is required.

7.3.6 V_O Current Protection

The LDO has a constant overcurrent limit (OCL).

7.3.7 V_{IN} UVLO Protection

For V_{IN}/VDD undervoltage lockout (UVLO) protection, the TPS7H3301-SP monitors V_{IN}/VDD voltage. When the V_{IN}/VDD voltage is lower than the UVLO threshold voltage, both the VTT and VTTREF regulators are powered off. This shutdown is a non-latch protection.

7.3.8 Thermal Shutdown

The TPS7H3301-SP monitors its junction temperature. If the device junction temperature exceeds its threshold value, (typically 210°C), the V_O/VTT and VTTREF regulators are both shutoff and discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

7.4 Device Functional Modes

The TPS7H3301-SP 3-A sink and source LDO provides low output noise to meet system needs. In order to improve efficiency in the LDO, TPS7H3301-SP LDO can operate from low VLDOIN voltage rail, thus using dual voltage source one for the VLDOIN that supports high-current and an alternate voltage source that provides voltage for VDDQSNS pin.

Typcically VLDOIN and VDDQSNS pins are tied together. In the memory system, VDDQ is a high-current supply that powers the core, the I/O, and the logic of the memory. VTTREF is a low-current, precision reference voltage that provides a threshold between a logic high (one) and a logic low (zero) that adapts to changes in the I/O supply voltage. By providing a precision threshold that adapts to the supply voltage, VTTREF realizes wider noise margins than those possible with a fixed threshold and normal variations in termination and drive impedance. Specifications vary from device manufacturer to manufacturer, but the most common specification is 0.49 to 0.51 times VDDQ and draws only tens to hundreds of microamps. The TPS7H3301-SP VTTREF is designed to sink and source at 10 mA.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7H3301-SP device is a highly-integrated sink and source LDO. The device is targeted to support VTT voltage for DDR memory applications and is capable of sourcing and sinking 3-A load current. The TPS7H3301-SP user's guide is available on www.ti.com, SLVUAK2. The guide highlights standard EVM test results, schematic, and bill of materials (BOM) for reference.

8.2 Typical Application

The design example describes a 2.5-V V_{IN}, DDR3 configuration.

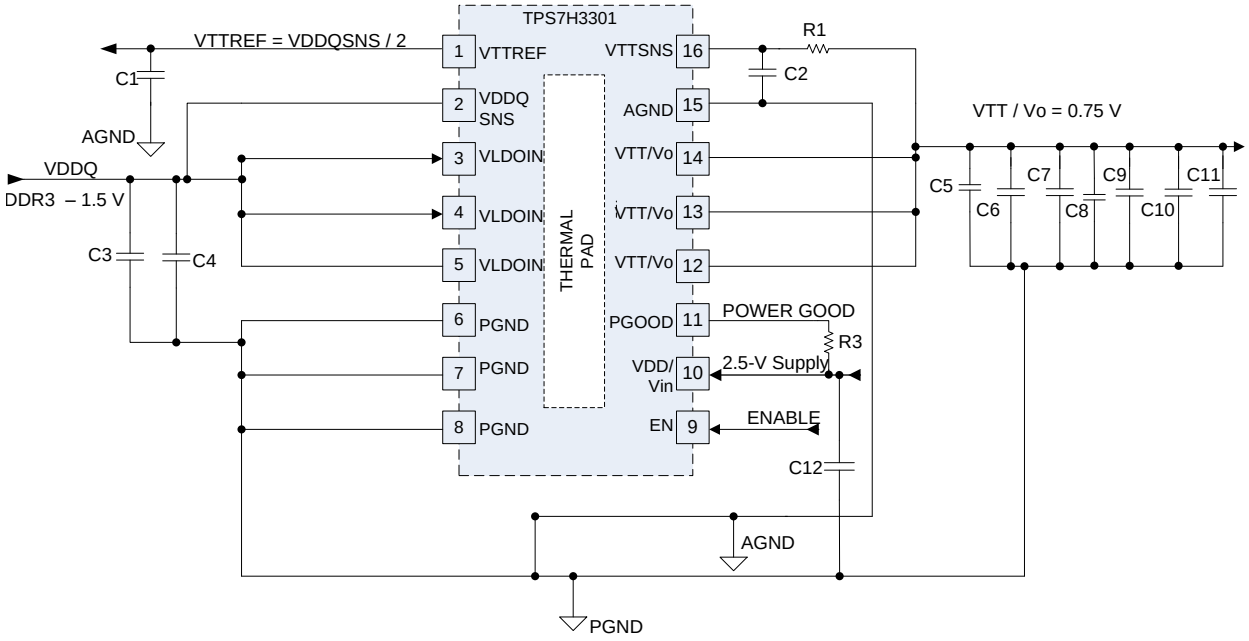


Figure 14. Typical Application Circuit

8.2.1 Design Requirements

See the *Recommended Operating Conditions* for recommended limits.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Table 1. Design Example 1 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1	Resistor	392 Ω	CRCW0603392RFKEA	
R3		100 kΩ	CRCW0603100KJNEA	
C3, C5, C6, C7	Capacitor	150 µF, 10 V	T530D157M010ATE005	Kemet
C2		1000 pF	GRM188R71H102KA01D	MuRata
C1		0.1 µF	08053C104KAT2A	AVX
C4, C8, C9, C10, C11		4.7 µF, 10 V	1210ZC475KAT2A	Murata
C12		10 µF, 10 V	GRM21BR71A106KE51L	Murata

8.2.2.1 V_{IN}/VDD Capacitor

Add a ceramic capacitor, with a value between 1- and 10-µF, placed close to the V_{IN}/VDD pin, to stabilize the bias supply (2.5-V rail or 3.3-V rail) from any parasitic impedance from the supply.

8.2.2.2 VLDO Input Capacitor

Depending on the trace impedance between the VLDOIN/VDDQ bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN/VDDQ input capacitor. Use a 150-µF (or greater) tantalum capacitor in parallel with a 4.7-µf ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VTT/V_O.

8.2.2.3 VTT Output Capacitor

For stable operation, the total capacitance of the VTT/V_O output pin must be greater than 470 µF. Attach three, 3 × 150-µF low-ESR tantalum capacitors in parallel with ceramic capacitors to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the ESR is greater than 2 mΩ, insert an R-C filter between the output and the VTTSNS input to achieve loop stability. The R-C filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

8.2.2.4 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin (VTTSNS) should be connected to the positive pin of the VTT pin output capacitor or capacitors as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor or capacitors is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

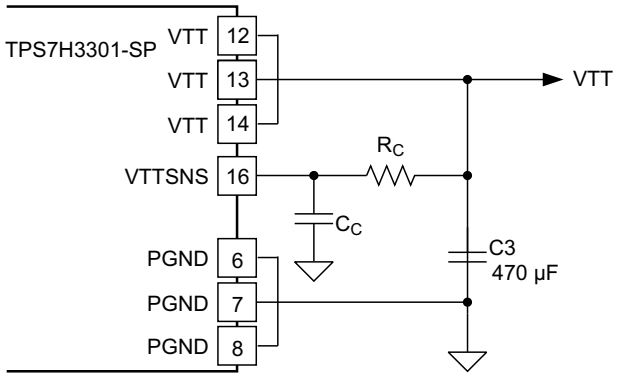


Figure 15. R-C Filter for VTTSNS

8.2.2.5 Low V_{IN} Applications

TPS7H3301-SP can be used in an application system where either a 2.5-V rail or a 3.3-V rail is available. The TPS7H3301-SP minimum input voltage requirement is 2.375 V. If a 2.5-V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is 2.375 V or greater. The voltage tolerance for a 2.5-V rail input is between –5% and 5% accuracy, or better.

8.2.2.6 S3 and Pseudo-S5 Support

The TPS7H3301-SP provides S3 support by an EN function. The EN pin could be connected to an SLP_S3 signal in the end application. Both VTTREF and V_O/VTT are on when EN = high (S0 state). VTTREF is maintained while V_O/ VTT is turned off and discharged via an internal discharge MOSFET when EN = low (S3 state). Please notice that the EN signal controls only the output buffer for V_O/VTT and therefore, while in S3 state, VDDQSNS is present in order to maintain data in volatile memory. As a result, when EN is set high to exit the S3 state, it is desired to bring V_O/VTT into regulation as fast as possible. This causes an output current controlled by the current limit of the device and the output capacitors.

When EN = low and the VDDQSNS voltage is less than 0.78 V, TPS7H3301-SP enters pseudo-S5 state. Both V_O/VTT and VTTREF outputs are turned off and discharged to GND through internal MOSFETs when pseudo-S5 support is engaged (S4/S5 state). Figure 16 shows a typical startup and shutdown timing diagram for an application that uses S3 and pseudo-S5 support.

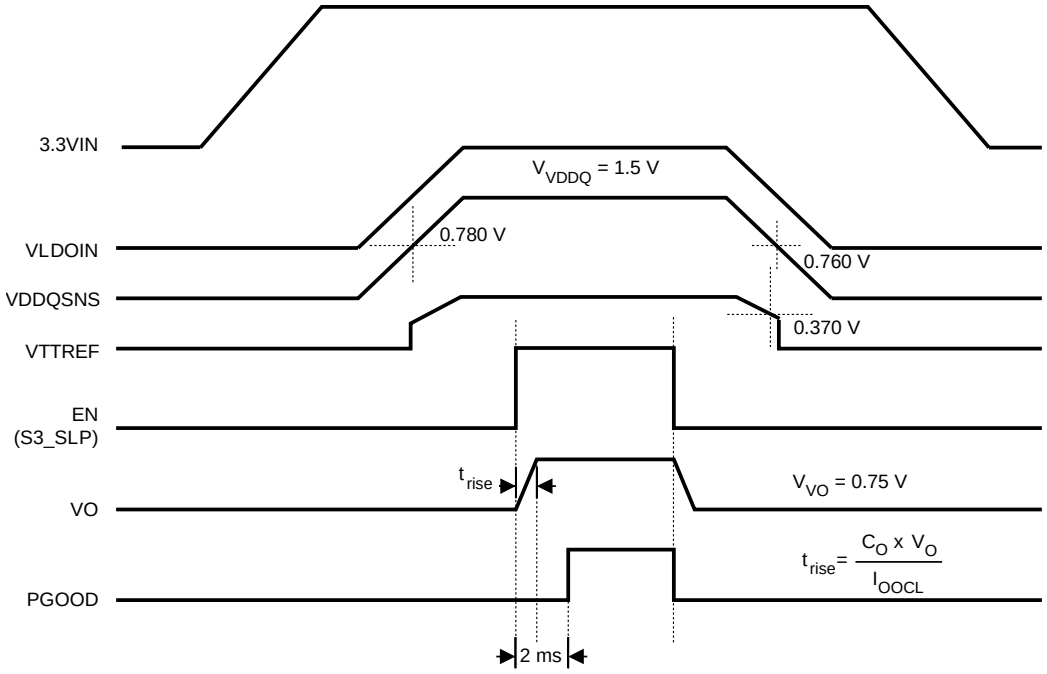


Figure 16. Typical Timing Diagram for S3 and Pseudo-S5 Support

8.2.2.7 Tracking Startup and Shutdown

The TPS7H3301-SP supports tracking startup of VDDQ and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, V_O/VTT follows VTTREF once VDDQSNS voltage is greater than 0.78 V. VDDQSNS incorporates a resistor divider network and a time constant of about 445 µs. The rise time of the V_O/VTT output is then a function of the rise time of the VDDQ rail if the VDDQ rise time is larger than 445 µs. PGOOD is asserted 2 ms after V_O/VTT is within ±20% of VTTREF. During tracking shutdown, V_O/VTT falls following VTTREF until VTTREF reaches 0.37 V. Once VTTREF falls below 0.37 V, the internal discharge MOSFETs are turned on and quickly discharge both VTTREF and V_O/VTT to GND. PGOOD is deasserted once V_O/VTT is beyond the ±20% range of VTTREF. Figure 17 shows the typical timing diagram for an application that uses tracking startup and shutdown.

There are no sequencing requirements between V_{IN}/VDD and VLDOIN. If VLDOIN is applied first followed by V_{IN}/VDD there is no issue. V_{IN} UVLO protection monitors V_{IN}/VDD voltage when V_{IN}/VDD is lower than UVLO threshold both VTT and VTTREF regulators are powered off.

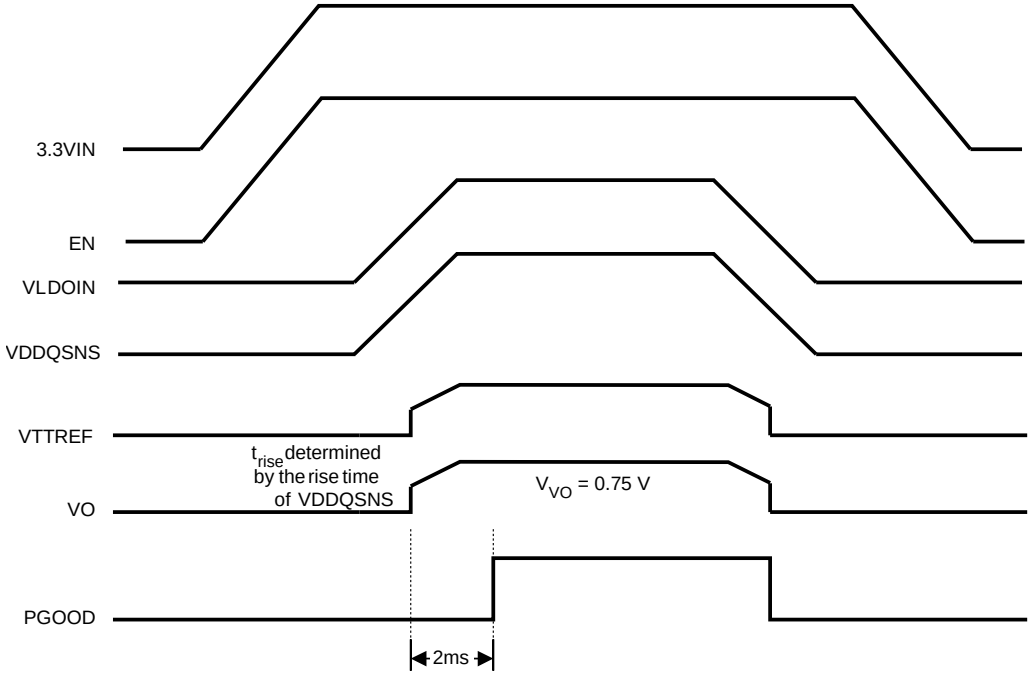


Figure 17. Typical Timing Diagram of Tracking Startup and Shutdown

8.2.2.8 Output Tolerance Consideration for VTT DIMM Applications

The TPS7H3301-SP is specifically designed to power up the memory termination rail (as shown in Figure 18). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 19 for typical characteristics for a single memory cell.

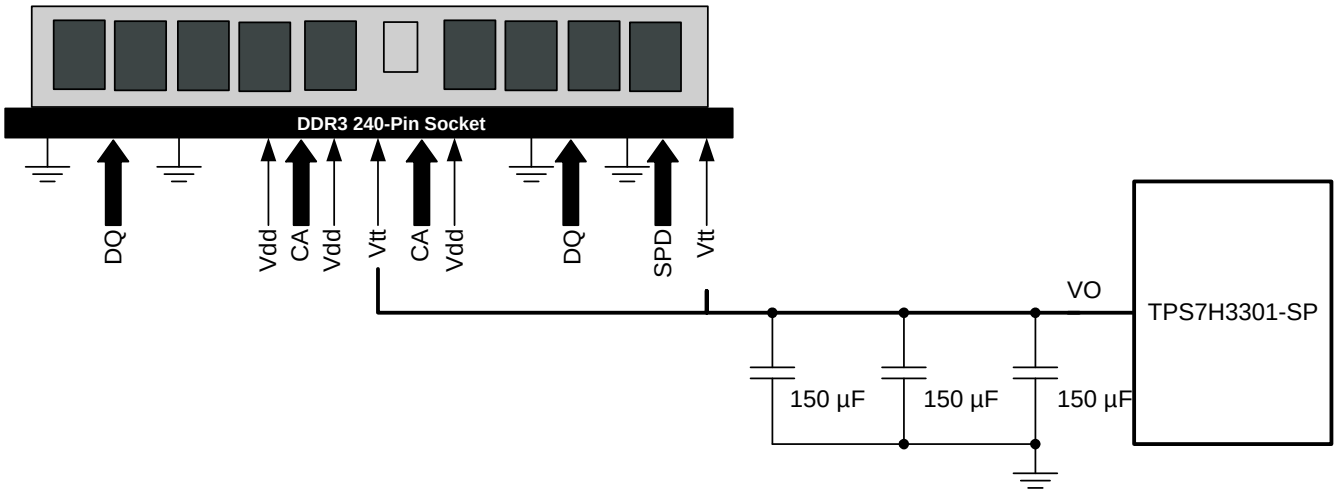


Figure 18. Typical Application Diagram for DDR3 VTT DIMM using TPS7H3301-SP

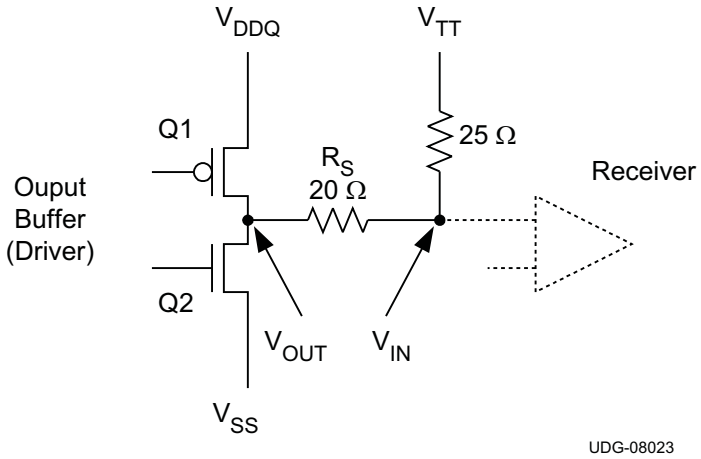


Figure 19. DDR Physical Signal System Bidirectional SSTL Signaling

In Figure 19, when Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT.
- VTT sinks current.

In Figure 19, when Q2 is on and Q1 is off:

- Current flows from VTT via the termination resistor to GND.
- VTT sources current.

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Based on JEDEC VTT specifications for DDR and DDR2 (JEDEC standard: DDR JESD8-9B May 2002; DDR2 JESD8-15A Sept 2003):

VTTREF – 40 mV < VTT < VTTREF + 40 mV, for both DC and AC conditions

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning.

The TPS7H3301-SP ensures the regulator output voltage to be:

VTTREF – 34 mV < VTT < VTTREF + 34 mV, for both DC and AC conditions and –3 A < I_{VTT} < 3 A

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3 and low-power DDR3/DDR4 applications (see Table 2 for detailed information). To meet the stability requirement, a minimum output capacitance of 470 µF is needed, combination of both tantalum and ceramic capacitors. Considering the actual tolerance on the MLCC capacitors, four or higher 4.7-µF ceramic capacitors in parallel with 3 × 150-µF low-ESR tantalum capacitor are sufficient to meet the above requirement. Higher ESR tantalum capacitors will require multiple tantalum capacitors in parallel with ceramic capacitors to meet system needs.

Table 2. DDR, DDR2, DDR3, and LP DDR3 Termination Technology and Their Differences

	DDR	DDR2	DDR3	LOW POWER DDR3 (DDR3L)
FSB data rates	200, 266, 333 and 400 MHz	400, 533, 677 and 800 MHz	800, 1066, 1330 and 1600 MHz	Same as DDR3
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT termination for address, command and control signals.	On-die termination for data group. VTT termination for address, command and control signals.	Same as DDR3
Termination current demand	Max sink and source transient currents of up to 2.6 A to 2.9 A	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1 A of burst current	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1 A of burst current	Same as DDR3
Voltage level	2.5-V core and I/O 1.25-V VTT	1.8-V core and I/O 0.9-V VTT	1.5-V core and I/O 0.75-V VTT	1.35-V core and I/O 0.68-V VTT

The TPS7H3301-SP is designed as a Gm-driven LDO. The voltage droop between the reference input and the output regulator is determined by the transconductance and output current of the device. The typical Gm is 250 S at 3 A and changes with respect to the load in order to conserve the quiescent current (that is, the Gm is very low at no load condition). The Gm LDO regulator is a single pole system. Its unity gain bandwidth for the voltage loop is only determined by the output capacitance, as a result of the bandwidth nature of the Gm (see Equation 1).

$$F_{UGBW} = \frac{Gm}{2 \times \pi \times C_{OUT}} \quad (1)$$

where

- F_{UGBW} is the unity gain bandwidth
- Gm is transconductance
- C_{OUT} is the output capacitance

There are two limitations to this type of regulator when it comes to the output bulk capacitor requirement. To maintain stability, the zero location contributed by the ESR of the output capacitors should be greater than the –3-dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design. In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the Gm –3-dB point because of the large ESL, the output capacitor, and parasitic inductance of the V_O trace.

Figure 20 shows the bode plot simulation for a typical DDR3 configuration of the TPS7H3301-SP, where:

- V_{IN} = 2.4 V
- V_{VLDOIN} = 1.5 V
- V_{VO} = 0.75 V
- I_{IO} = 2 A
- 3 × 150-µF low-ESR tantalum capacitors (T530D157M010ATE005) in parallel with 4 × 4.7-µF ceramic capacitor
- ESR = 1.66 mΩ
- ESL = 800 pH

The unity-gain bandwidth is approximately 87.3 kHz and the phase margin is 82°. The 0-dB level is crossed, the gain peaks because of the ESL effect. However, the peaking is kept well below 0 dB.

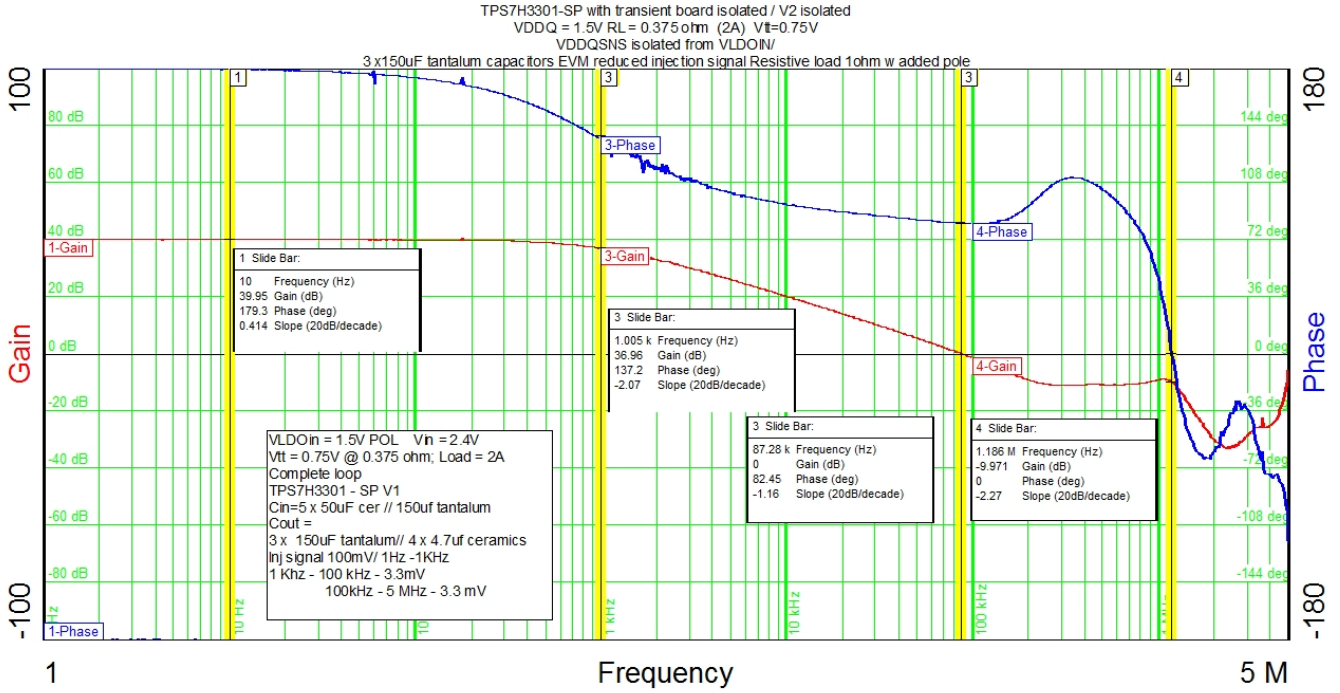


Figure 20. Bode Plot for a Typical DDR3 Configuration

Figure 3 shows the load regulation and Figure 21 shows the transient response for a typical DDR3 configuration. When the regulator is subjected to ±1.5-A load step and release, the output voltage measurement shows no difference between the DC and AC conditions.

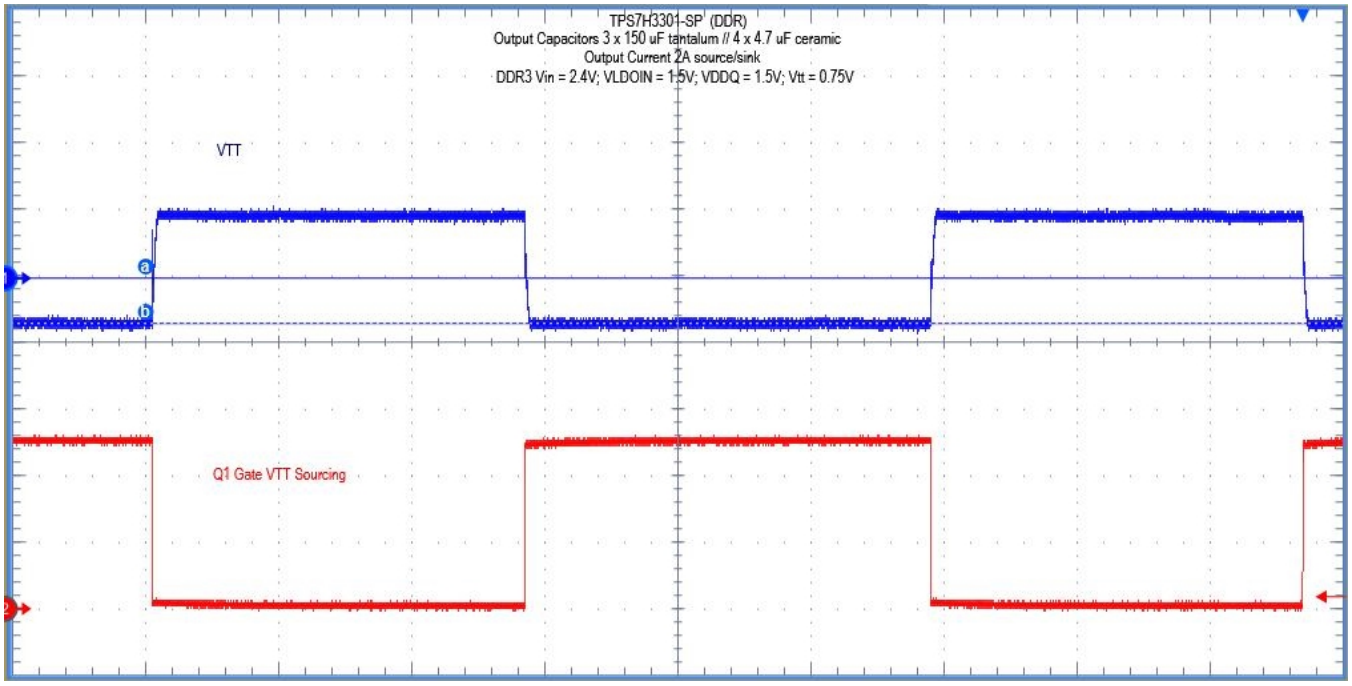


Figure 21. Transient Plot

8.2.2.9 LDO Design Guidelines

The minimum input (VLDOIN) to output voltage (V_O/V_{TT}) difference (headroom) decides the lowest usable supply voltage Gm-driven to drive a certain load. For TPS7H3301-SP, a minimum of 300 mV ($VLDOIN_{MIN} – V_{OMAX}$) is needed in order to support a Gm driven sourcing current of 3 A based on a design of V_{IN} = 3.3 V and C_{OUT} = 470 µF. Because the TPS7H3301-SP is essentially a Gm-driven LDO, its impedance characteristics are both a function of the 1/Gm and $R_{DS(on)}$ of the sourcing MOSFET (see Figure 22). The current inflection point of the design is between 3 A and 4 A. When I_{SRC} is less than the inflection point, the LDO is considered to be operating in the Gm region; when I_{SRC} is greater than the inflection point but less than the overcurrent limit point, the LDO is operating in the $R_{DS(on)}$ region. The typical sourcing $R_{DS(on)}$ is 154 mΩ with V_{IN} = 3 V and T_J = 125°C.

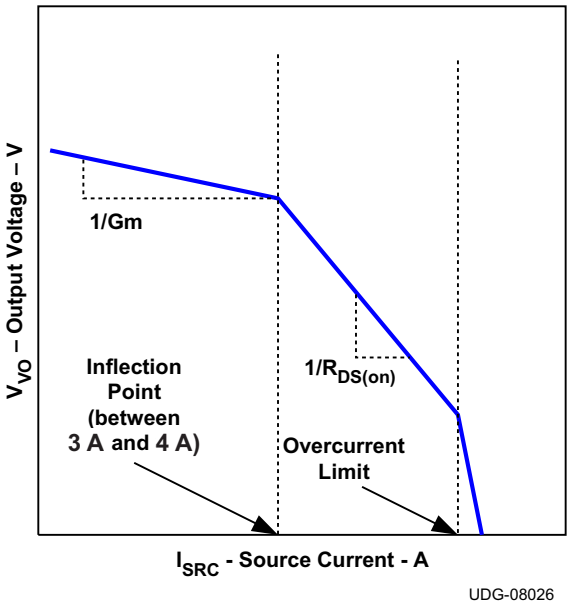


Figure 22. TPS7H3301-SP Impedance Characteristics

8.2.3 Application Curve

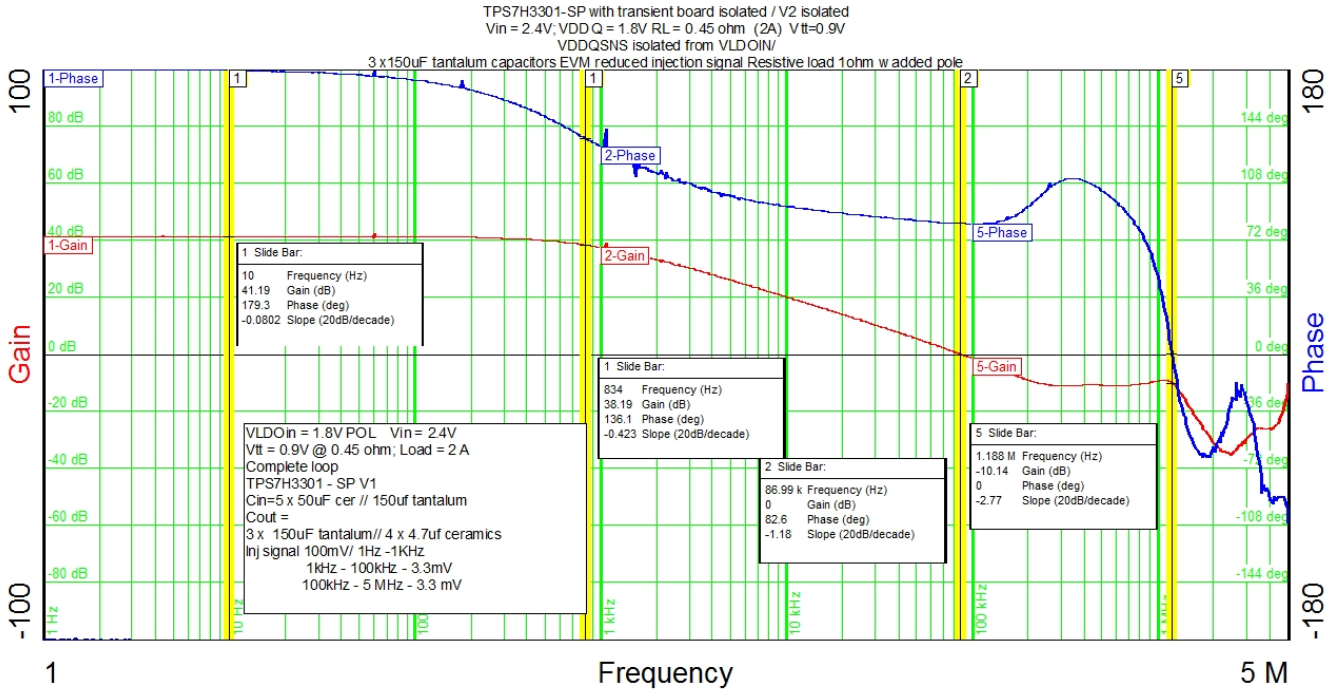


Figure 23. DDR2 2-A Load V_{IN} = 2.4 V, VTT = 0.9 V

9 Power Supply Recommendations

TPS7H3301-SP is designed to support DDR, DDR2, DDR3, DDR3L, and DDR4 VTT applications. TPS7H3301-SP VLDOIN supports voltage range from 0.9 V to 3.5 V. The supply must be well regulated. Having a separate VLDOIN and VDDQSNS allows designer to optimize system efficiency. V_{IN}/VDD is used to bias the TPS7H3301-SP IC and its voltage range from 2.375 V to 3.5 V. This supply must be well regulated and bypassed with a ceramic capacitor with a value of 1 µF and 10 µF. TI recommends that VLDOIN and VDDQSNS be isolated from each other. If this is not possible then an RC filter must be used to isolate VLDOIN and VDDQNSS. However, in so doing the dynamic tracking of VTT and VTTREF will be lost. See the user's guide SLVUAK2 for additional details.

10 Layout

10.1 Layout Guidelines

Consider the following points before starting the TPS7H3301-SP layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for V_O/VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VOSNS should be connected to the positive node of V_O/VTT output capacitors as a separate trace from the high-current power line. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor or capacitors at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor or capacitors.
- Consider adding low-pass filter at VOSNS if the ESR of the V_O/VTT output capacitor or capacitors is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise-generating lines.
- The negative node of the V_O/VTT output capacitor or capacitors and the VTTREF capacitor should be tied together by avoiding common impedance to the high-current path of the V_O/VTT sink and source current.
- The GND and PGND pins should be connected to the thermal land underneath the die pad with multiple vias connecting to the internal system ground planes (for better result, use at least two internal ground planes). Use as many vias as possible to reduce the impedance between PGND/GND and the system ground plane. Also, place bulk caps close to the DIMM load point and route the VOSNS to the DIMM load sense point.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package's thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias, 0.33 mm in diameter, connected from the thermal land to the internal/solder side ground plane or planes should also be used to help dissipation.

10.2 Layout Example

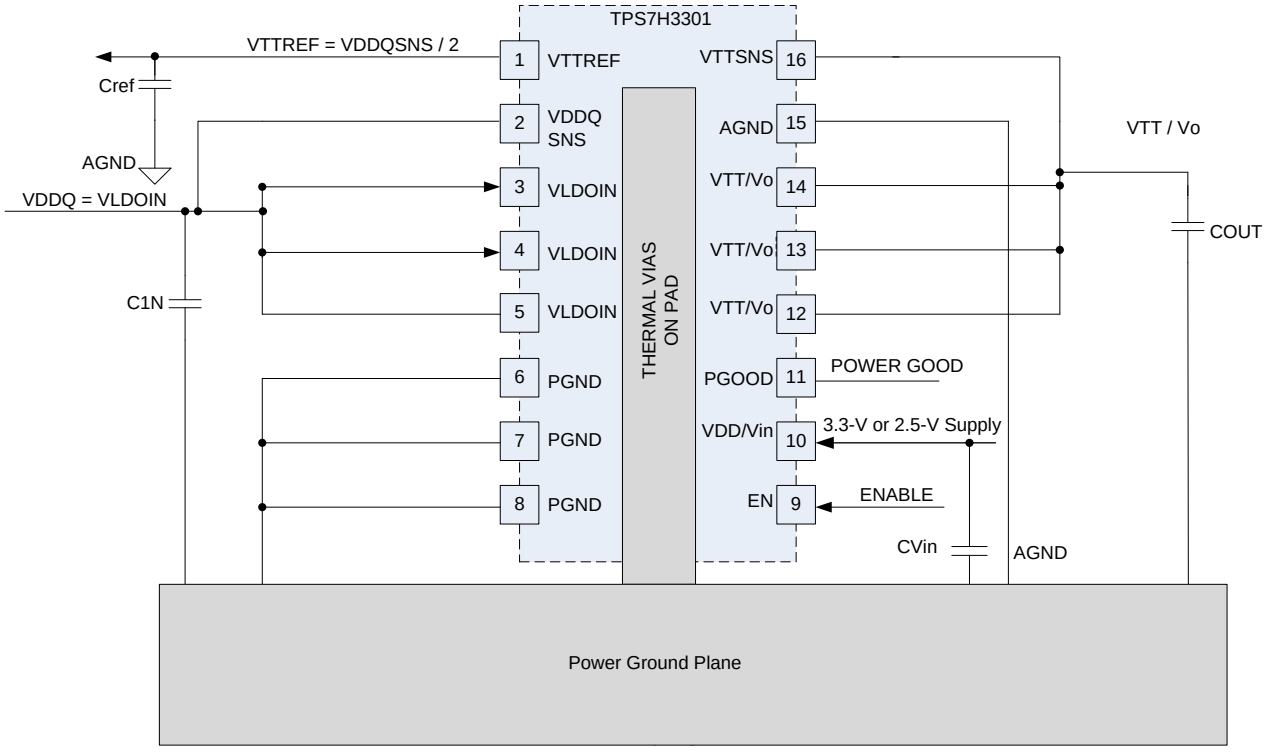


Figure 24. Layout Recommendation

10.3 Thermal Considerations

Because the TPS7H3301-SP is a linear regulator, the V_O current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between VLDOIN and V_O times IO (I_{IO}) current becomes the power dissipation as shown in Equation 2.

$$P_{DISS\_SRC} = (V_{VLDOIN} - V_{VO}) \times I_{O\_SRC} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, V_O voltage is applied across the internal LDO regulator and the power dissipation (P_{DISS_SNK}) can be calculated by Equation 3.

$$P_{DISS\_SNK} = V_{VO} \times I_{O\_SNK} \quad (3)$$

Because the device does not sink and source current at the same time and the IO current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry from the V_{IN} supply and the VLDOIN supply. This can be estimated as 5 mW or less during normal operating conditions. This power must be effectively dissipated from the package.

The thermal performance of an LDO depends on the printed circuit board (PCB) layout. Because the TPS7H3301-SP device is shipped unformed, only the recommended heat pad pattern is shown. Lead pad placement depends on final form factor.

To further improve the thermal performance of this device, using a larger than recommended thermal land as well as increasing the number of vias helps lower the thermal resistance from junction to heat slug. TI recommends that up to 48 (0.01 in) thermal vias can be located under the device package.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1422801VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962-1422801VXC TPS7H3301-SP	Samples
5962R1422801VXC	ACTIVE	CFP	HKR	16	1	TBD	NIAU	N / A for Pkg Type	-55 to 125	5962R1422801VXC TPS7H3301-RHA	Samples
TPS7H3301HKR/EM	ACTIVE	CFP	HKR	16		TBD	NIAU	N / A for Pkg Type	25 only	TPS7H3301HKREM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

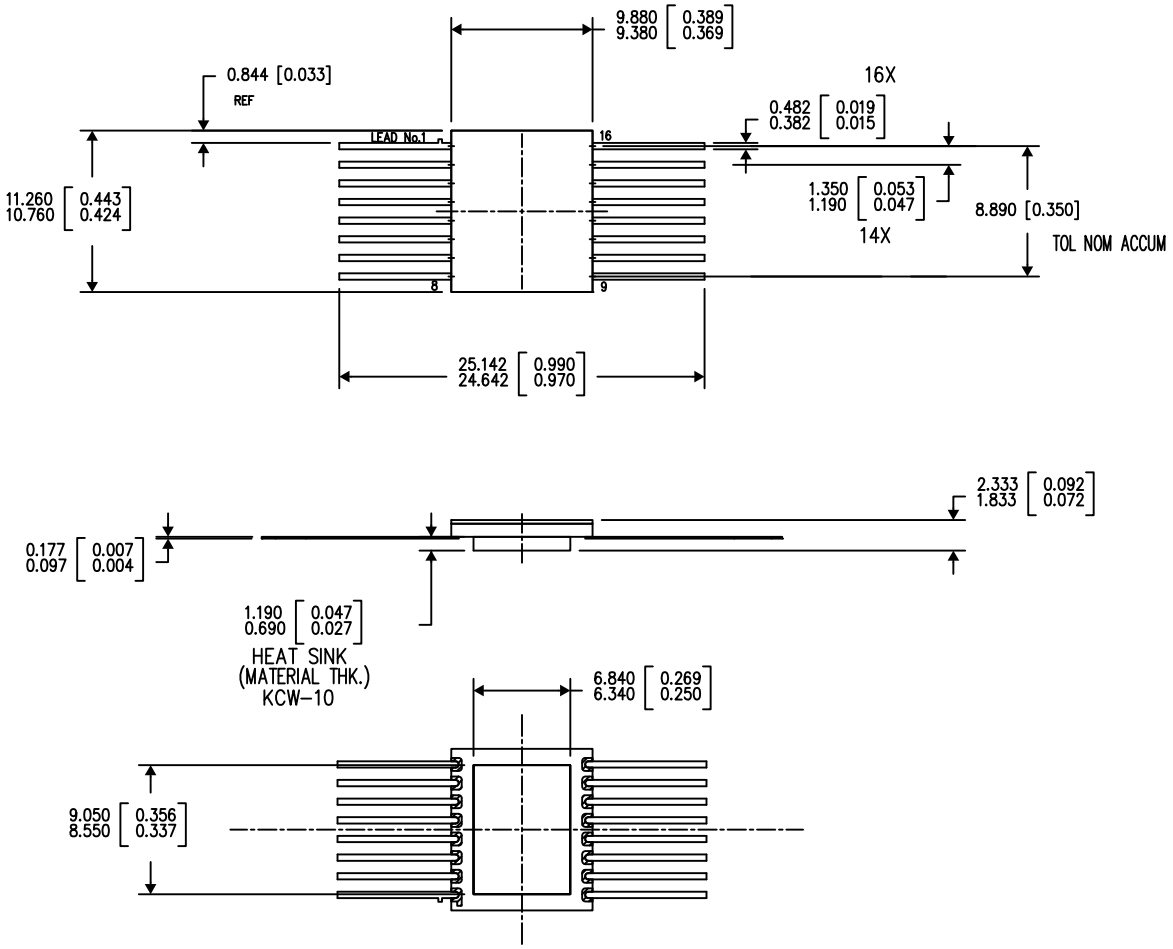
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

HKR (R–CDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid. Lid and heat slug are connected to pin 8 (Gnd).
D. The terminals will be gold plated.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265